Patent Claims

1. An integrated circuit arrangement (10),
having at least one metallization layer (16) containing a multiplicity of electrically conductive interconnects (14),
having an interconnect dielectric (18) between the interconnects (14),
having electrically conductive interconnect intermediate material (20) arranged in each case between a side area (40) of an interconnect (14) and the interconnect dielectric (18),
having a multiplicity of electrically conductive connecting sections (12) which in each case form a section of an electrically conductive connection to or from an interconnect (14),
having a connecting section dielectric (24) between the connecting sections (12),
having connecting section intermediate material (28) arranged in each case between a connecting section (12) and the connecting section dielectric (24) and/or between a connecting section (12) and an interconnect (14),
the interconnect intermediate material (20) and the connecting section intermediate material (28) making contact with one another at at least one connection (12).

2. The circuit arrangement (10) as claimed in claim 1, wherein, at the connection, the interconnect intermediate material (20) and the connecting section intermediate material (28) make contact at two or three or four side areas (40) of an interconnect (14)
and/or wherein the interconnect intermediate material (20) and the connecting section intermediate material (28) make contact at an edge (42) formed by the contact line of two side areas of the interconnect (14).

3. The circuit arrangement (10) as claimed in claim 1 or 2, wherein the interconnect (14) has a constriction (72, 82, 112, 132) at the connecting section (12), the width (B3, B4, B7, B8) of said constriction being chosen such that contact regions are produced at opposite side areas of the interconnect (14),
and/or wherein the constriction (72, 112), along the longitudinal axis of the interconnect (14), has a length (L1, L2) that is less than five times or less than three times the width (B3, B7) of the constriction (72, 112).

4. The circuit arrangement (10) as claimed in claim 3, wherein the connecting section (12) is arranged at the end of the interconnect (14),
and/or wherein the constriction (112, 132) has the form of a wedge or the form of a step.

5. The circuit arrangement (10) as claimed in claim 3, wherein the interconnect (14) extends in at least two different directions from the connecting section (12),
and/or wherein the constriction (72, 82), at its ends, in each case has the form of a wedge or the form of a step.

6. The circuit arrangement (10) as claimed in claim 1 or 2, wherein at least two sections of the same interconnect (14) or of different interconnects are wider than the connecting sections (12) at connecting sections (12),
and wherein the contact regions are situated at such side areas of the sections whose normal directions are situated transversely or oppositely with respect to one another.

7. The circuit arrangement (10) as claimed in one of the preceding claims, wherein the interconnect (14)

comprises copper or a copper alloy containing at least ninety-five percent copper,
and/or wherein the interconnect (14) comprises aluminum or an aluminum alloy containing at least ninety-five percent aluminum,
and/or wherein the interconnect dielectric (18) and/or the connecting section dielectric contains an oxide, preferably silicon dioxide, or a dielectric having a dielectric constant of less than 3.9,
and/or wherein the interconnect intermediate material (20) and/or the connecting section intermediate material (28) contains a nitride, preferably comprises a nitride, in particular made of a metal nitride,
and/or wherein the interconnect intermediate material contains a refractory metal or comprises a refractory metal, preferably made of tantalum,
and/or wherein the connecting sections (12) contain tungsten, preferably comprise tungsten, or wherein the connecting sections (12) contain copper or comprise copper.

8. The circuit arrangement (10) as claimed in one of the preceding claims, wherein the area of an interconnect (14) that is adjacent to a connecting section (12) is essentially free and/or more than eighty percent free of an electrically conductive intermediate material,
and/or wherein the circuit arrangement (10) has been fabricated by means of a damascene technique or by means of a dual damascene technique.

9. A method for generating design data for the production of an integrated circuit arrangement (10), in particular of a circuit arrangement (10) as claimed in one of the preceding claims,
having the steps that are performed without restriction by the order specified and with the aid of an apparatus (200):

predefinition (304) of design data that determine the geometrical arrangement of interconnects (14) in a metallization layer (16) and of connecting sections (12) which in each case form a section of an electrically conductive connection to or from an interconnect (14),

predefinition (304) of at least one rule for altering the design data, the application of the rule to the design data giving rise to changed design data that determine a changed arrangement of interconnects (14) and connecting sections (12), and the number of contact locations of interconnect intermediate material (20) between an interconnect (14) and an interconnect dielectric (18) and of connecting section intermediate material (28) between a connecting section (28) and a connecting section dielectric (18) being increased in a targeted manner in comparison with the original arrangement by application of the rule,

automatic application (310) of the rule to the design data, the changed design data being generated,

outputting (316) and/or storage of the changed design data.

10. The method as claimed in claim 9, wherein in accordance with one rule, the width of a pattern for an interconnect (14), in particular in an overlap region with a pattern for a connecting section (12), is reduced, preferably in wedge-shaped or stepped fashion, and/or wherein, in accordance with another rule, a pattern for an interconnect (14) and/or a pattern for a connecting section (12) is displaced in a design plane.

11. A program (354) having an instruction sequence whose execution by a data processing system (320) has the effect of performing a method as claimed in claim 9 or 10.

12. An apparatus (320), in particular a data

processing system, for generating design data, in particular according to a method as claimed in claim 9 or 10,

having an access unit for accessing design data that determine the geometrical arrangement of interconnects (14) in a metallization layer (16) and of connecting sections (12) which in each case form a section of an electrically conductive connection to or from an interconnect (14),

having a unit (324) which stores at least one rule for altering the design data, the application of the rule to the design data giving rise to changed design data that determine a changed arrangement of interconnects (14) and connecting sections (12), and the number of contact locations of interconnect intermediate material (20) between an interconnect (14) and an interconnect dielectric (18) and of connecting section intermediate material (28) between a connecting section (28) and a connecting section dielectric (18) being increased in a targeted manner in comparison with the original arrangement by application of the rule,

and having a processing unit (326, 328), which automatically applies the rule to the design data, the changed design data being generated.